

CLAIMS

WHAT IS CLAIMED IS:

- 1 1. A method of manufacturing an integrated circuit, comprising:
2 providing a gate structure between a source location and a drain
3 location in a semiconductor substrate;
4 providing an angled source extension implant in a direction from the
5 source location to the drain location;
6 providing an angled drain extension implant in a direction from the
7 drain location to the source location; and
8 providing a deep source/drain implant at the source location and the
9 drain location.
- 1 2. The method of claim 1, further comprising providing a pair of
2 spacers abutting lateral sides of the gate structure before the deep source drain
3 implant.
- 1 3. The method of claim 2, wherein the providing the source
2 extension step is a low energy, high dose ion implantation step.
- 1 4. The method of claim 3, wherein the drain extension implant step
2 is a medium energy, high dose ion implantation step.
- 1 5. The method of claim 4, wherein a source extension formed by the
2 source extension step is shallower than a drain extension formed by the drain
3 extension implant step.
- 1 6. The method of claim 5, wherein the source extension has
2 approximately 5 times the concentration of dopants of the drain extension.
- 1 7. The method of claim 5, wherein the source extension has a
2 concentration of 5×10^{19} - 1×10^{20} of dopants per centimeter cubed and the drain
3 extension has a concentration of 1×10^{19} - 5×10^{19} dopants per centimeter cubed.

1 8. The method of claim 5, wherein the drain extension has a
2 concentration between 1×10^{19} - 5×10^{19} dopants per centimeter cubed.

1 9. The method of claim 5, wherein the drain extension is more than
2 80 nm deep.

1 10. The method of claim 7, wherein the gate structure is associated
2 with a N-channel or P-channel with MOSFET.

1 11. A method of manufacturing an ultra-large scale integrated circuit
2 including a plurality of field effect transistors, the method comprising steps of:

3 providing at least part of a gate structure on a top surface of a
4 semiconductor substrate;

5 forming a source extension with dopants of a first conductivity type;

6 forming a drain extension with dopants of the first conductivity type;

7 and

8 forming deep source and drain regions with dopants of the first
9 conductivity type, wherein the gate structure is between the source and drain
10 regions, wherein the drain extension is deeper than the source extension.

1 12. The method of claim 11, wherein the forming source and drain
2 regions further comprises:

3 providing a pair of spacers abutting lateral sides of the gate structure;

4 and

5 providing a deep source/drain implant at the source location and the
6 drain location.

1 13. The method of claim 11, wherein the drain extension is formed
2 in a low dosage implant process.

1 14. The method of claim 11, wherein the source extension is formed
2 at an energy level of between 1-5 KeV.

1 15. The method of claim 11, wherein the drain extension is formed
2 at an energy level of between 5-15 KeV.

3 16. The method of claim 11, wherein the first conductivity type is
4 N-type.

5 17. The method of claim 11, wherein the first conductivity type is P-
6 type.

1 *note*
2 18. An integrated circuit including a plurality of field effect
3 transistors, each of the transistors comprising:
4 a gate structure disposed over a channel;
5 a deep source region heavily doped with dopants of a first
6 conductivity type;
7 a deep drain region heavily doped with dopants of the first
8 conductivity type;
9 a source extension integral the deep source region; and
10 a drain extension integral the deep drain region, wherein the drain
extension is deeper than the source extension.

1 19. The integrated circuit of claim 18, wherein the source extension
2 is more heavily doped than the drain extension.

1 20. The integrated circuit of claim of claim 19, wherein the drain
2 extension is more than 80 nm thick and the source extension is less than 40 nm
3 thick.

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